What is Claimed is:

1. A fast Fourier transform processor for demodulating an orthogonal frequency division multiplexing signal having a symbol, the symbol including a first long preamble and first data, the fast Fourier transform processor comprising:

a timing acquisition section that is configured to output a timing signal in response to detect an end point of the first long preamble;

a controller that is configured to output a first control signal and a second control signal in response to the timing signal;

a signal converter that is configured to store the first long preamble in response to the first control signal, to transform the first long preamble by a fast Fourier transform into a second long preamble, to store the second long preamble, to transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, to store the second data, and to output the second data; and

a frequency domain equalizer that is configured to synchronize the second long preamble and the second data that is output from the signal converter in response to the second control signal with a clock frequency of the fast Fourier transform processor, and to output the synchronized second long preamble and second data.

2. The fast Fourier transform processor according to Claim 1, wherein the signal converter includes:

an input buffer that is configured to temporarily store the first data in response to the first control signal, and to output the temporarily stored first data;

a memory bank that is configured to store the first long preamble and the first data, to store the second long preamble and the second data, and to output the stored first and second long preamble and the stored first and second data in response to the first control signal; and

a frequency converter that is configured to read the first long preamble stored in the memory bank in response to the first control signal, to transform the first long preamble into a second long preamble in a frequency domain, to store the second long preamble in the memory bank, to transform the first data provided from the input buffer and the first data directly input to the frequency converter into second data in the frequency domain in response to the first control signal, and to store the second data in the memory bank.

3. The fast Fourier transform processor according to Claim 2, wherein the memory bank includes first, second, third and fourth memories.

4. The fast Fourier transform processor according to Claim 2, wherein the input buffer has a single port and stores N/2-samples of the symbol that is input.

5. The fast Fourier transform processor according to Claim 2, wherein the frequency converter includes a pipelined radix-2 FFT.

6. The fast Fourier transform processor according to Claim 2, wherein the memory bank is configured to receive the first and second long preambles and the first and second data and to output the first and second long preambles and the first and second data so that the memory bank performs an input function and an output function.

7. The fast Fourier transform processor according to Claim 3, wherein each of the first, second, third and fourth memories stores N/2-samples of the symbol.

8. A method of transforming an Orthogonal Frequency Division Multiplexing (OFDM) signal by a fast Fourier transform, the OFDM signal having a symbol, the symbol including a first long preamble, a second long preamble and first data, the first and second long preambles respectively having a sequence of N-samples, the method comprising:

(a) storing the first long preamble and the second long preamble in first, second, third and fourth memories in sequence as the OFDM signal is received;

(b) reading the first long preamble and the second long preamble stored in the first, second, third and fourth memories in response to an end point of the second long preamble being detected, transforming the first and second long preambles by a fast Fourier transform, respectively, into a third preamble and a fourth preamble, and storing in sequence the third and fourth long preambles in the first memory and the second memory;

(c) transforming second data that is input after first data is buffered, and the first data that is directly input, respectively, into third data when the first and second

long preambles are transformed into the third and fourth data, storing the third data in the memories in sequence, and outputting the third data stored in the memories; and

(d) finishing the fast Fourier transform method when the symbol is a final symbol, and performing (c) when the symbol is not the final symbol.

9. The method according to claim 8, wherein (c) comprises:

(c-1) activating a first toggle signal that is configured to control read and write operations with respect to the memories when the first long preamble and the second long preamble are transformed by the fast Fourier transform;

(c-2) determining whether or not the first data are transformed by the fast Fourier transform when the first toggle signal is in an active state;

(c-3) storing in sequence the third data in the first memory and the third memory when the first and second data are transformed by the fast Fourier transform, and outputting in sequence the third data stored in the second and fourth memories; and

(c-4) inverting the first toggle signal, and activating a second toggle signal for controlling the read and write operations with respect to the memories.

10. The method according to Claim 9, wherein (c-3) further includes storing in sequence the second data in the second memory and the fourth memory when the first data is transformed by the fast Fourier transform, and outputting in sequence the third data stored in the first memory and the third memory.

11. The method according to Claim 9, wherein the first toggle signal controls the read operation with respect to the first and third memories and controls the write operation with respect to the second and fourth memories, and the second toggle signal controls the write operation with respect to the first and third memories and controls the read operation with respect to the second and fourth memory.

12. The method according to Claim 8, wherein the first data is delayed data by N/2.

13. An Orthogonal Frequency Division Multiplexing (OFDM) receiver comprising:

a quadrature detector that is configured to receive an OFDM signal having a symbol, the symbol having a first long preamble and first data, to convert the OFDM signal into a baseband OFDM signal, to generate a real component of the OFDM signal and an imaginary component of the OFDM signal, and to output the real component of the OFDM signal and the imaginary component of the OFDM signal;

an A/D converter that is configured to convert the real and imaginary components of the OFDM signal, respectively, into digital real and imaginary components of a digital OFDM signal, and to output the digital real and imaginary components of the digital OFDM signal;

a fast Fourier transform processor that is configured to transform the digital OFDM signal by a fast Fourier transform; and

a demodulator that is configured to receive the transformed real and imaginary components of the transformed OFDM signal to demodulate the transformed real and imaginary components of the transformed OFDM signal;

wherein the fast Fourier transform processor comprises:

a timing acquisition section that is configured to output a timing signal in response to detecting an end point of the first long preamble;

a controller that is configured to output a first control signal and a second control signal in response to the timing signal;

a signal converter that is configured to store the first long preamble in response to the first control signal, to transform the first long preamble by a fast Fourier transform into a second long preamble, to store the second long preamble, to transform sequentially the first data by the fast Fourier transform into second data as the first data sequentially is received, to output the second long preamble, to store the second data, and to output the second data; and

a frequency domain equalizer that is configured to synchronize the second long preamble and the second data that is output from the signal converter in response to the second control signal with a clock frequency of the fast Fourier transform processor, and to output the synchronized second long preamble and second data.

14. The OFDM receiver according to Claim 13, wherein the signal converter includes:

an input buffer that is configured to temporarily store the first data in response to the first control signal, and to output the temporarily stored first data;

a memory bank that is configured to store the first long preamble and the first data, to store the second long preamble and the second data, and to output the stored first and second long preamble and the stored first and second data in response to the first control signal; and

a frequency converter that is configured to read the first long preamble stored in the memory bank in response to the first control signal, to transform the first long preamble into a second long preamble in a frequency domain, to store the second long preamble in the memory bank, to transform the first data provided from the input buffer and the first data directly input to the frequency converter into second data in the frequency domain in response to the first control signal, and to store the second data in the memory bank.

15. The OFDM receiver according to Claim 14, wherein the memory bank is configured to receive the first and second long preambles and the first and second data during a long preamble period so that the memory bank performs an input function, and to output the first and second long preambles and the first and second data during another period past the long preamble period so that the memory bank performs an output function.

16. The OFDM receiver according to Claim 14, wherein the memory bank includes first, second, third and fourth memories in which N/2 samples of the OFDM signal are stored, respectively.

17. The OFDM receiver according to Claim 14, wherein the input buffer includes a single port memory and receives N/2 samples.

18. A Fast Fourier Transform (FFT) processor for processing an Orthogonal Frequency Division Multiplexing (OFDM) signal having a symbol, the symbol including a first long preamble and first data, the FFT processor comprising:

an input buffer that is configured to temporarily store the first data;

a memory bank that is configured to store the first long preamble; and

an FFT unit that is configured to transform the first long preamble in the memory bank into a second long preamble in a frequency domain and to store the second long preamble back into the memory bank, to transform the first data that is

temporarily stored in the input buffer into second data in the frequency domain and to store the second data into the memory bank.

19. An FFT processor according to Claim 18 wherein the memory bank is configured to receive the first and second long preambles and the first and second data and to output the first and second long preambles and the first and second data so that the memory bank performs an input function and an output function.

20. A Fast Fourier Transform (FFT) method for processing an Orthogonal Frequency Division Multiplexing (OFDM) signal having a symbol, the symbol including a first long preamble and first data, the FFT method comprising:

temporarily storing the first data in an input buffer;

directly storing the first long preamble in a memory bank; and

transforming the first long preamble in the memory bank into a second long preamble in a frequency domain and storing the second long preamble back into the memory bank; and

transforming the first data that is temporarily stored in the input buffer into second data in the frequency domain and storing the second data into the memory bank.